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(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
4 April 2002 (04.04.2002)

PCT

(10) International Publication Number
WO 02/27783 A1

(51) International Patent Classification[7]: H01L 21/762, 21/20

(21) International Application Number: PCT/GB01/04321

(22) International Filing Date:
27 September 2001 (27.09.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/675,840 29 September 2000 (29.09.2000) US

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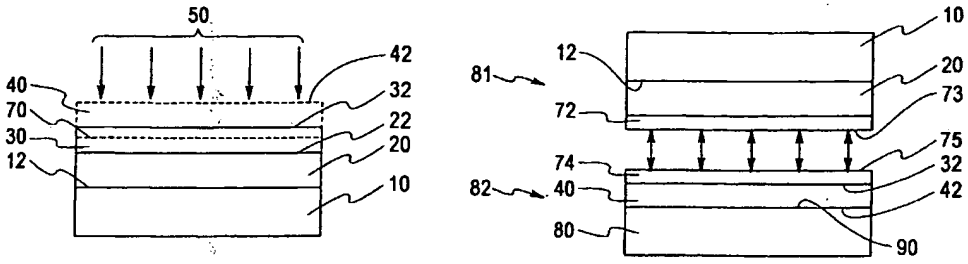
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: PREPARATION OF A RELAXED SiGe LAYER ON AN INSULATOR



(57) Abstract: A method for forming strained Si or SiGe on relaxed SiGe on insulator (74) (SGOI) is described incorporating growing a graded Si_{1-x} Ge_x layer (20) and an epitaxial Si_{1-y} Ge_y layer on a semiconductor substrate, implanting hydrogen (70) into said Si_{1-y} Ge_y layer (30) to form a hydrogen-rich defective layer, smoothing surfaces by Chemo-Mechanical Polishing, bonding two substrates together via thermal treatments and separating the two bonded substrates at the hydrogen-rich defective layer. The separated substrates may have its upper surface (75) smoothed by CMP for epitaxial deposition of further layer.

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PREPARATION OF A RELAXED SiGe LAYER ON AN INSULATOR

FIELD OF INVENTION

This invention relates to a method of preparing an SiGe layer on an insulator to provide a structure which is useful for fabricating high speed devices such as complementary metal-oxide-semiconductor (CMOS) transistors, modulation-doped field-effect-transistors (MODFETs), high electron mobility transistors (HEMTs) and bipolar transistors.

BACKGROUND OF THE INVENTION

Electron mobility in strained Si/SiGe channels is significantly higher than that in bulk Si. For example, measured values of electron mobility in strained Si at room temperature are about 3000 cm^2/Vs as opposed to 400 cm^2/Vs in bulk Si. Similarly, hole mobility in strained SiGe with high Ge concentration (60%~80%) reaches up to 800 cm^2/Vs, the value of which is about 5 times the hole mobility in bulk Si of 150 cm^2/Vs. The use of strained crystalline materials in state-of-the-art Si devices is expected to result in much higher performances, higher operating speeds in particular. Strained Si/SiGe is of particular significance when conventional Si devices continue to scale down to 0.1mm regime and start to approach the fundamental limits of unstrained materials.

However, the underlying conducting substrate for MODFETs and bipolar transistors or the interaction of the underlying substrate with the active device regions in CMOS are undesirable features which limit the full performance of high speed devices. To resolve the problem, in Si technology, an insulating layer is usually used to isolate the active device region from the substrate before creating Silicon-On-Insulator (SOI) materials to replace bulk Si material for device fabrication. Available technology to achieve SOI wafers includes Separation by Implanted Oxygen (SIMOX), bonding and etchback Silicon-On-Insulator (BESOI), separation by implanted hydrogen also known as the Smart-Cut® process which is described in U.S. Pat. No. 5,374,564 by M. Bruel which issued Dec. 20, 1994, or the combination of the last two processes for making ultra-thin SOI, U.S. Pat. No. 5,882,987 by K.V. Srikrishnan which issued Mar. 16, 1999.

When Si is substituted by strained Si/SiGe layers for high speed applications, there is a need for techniques capable of providing SiGe on insulator substrates or wafers for the fabrication of strained Si/SiGe on insulator materials. In U.S. Pat. No. 5,906,951 by Chu et al. which issued May 25, 1999, a method of utilizing wafer bonding and backside etching in KOH with a p^{++}-doped SiGe etch-stop to form a layer of strained Si/SiGe on a SOI substrate was described. However, the etch-stop layer is heavily doped by boron in the range from $5x10^{19}$ to $5x10^{20}$ atoms/cm^3 and therefore there are chances of the boron auto-doping the strained Si/SiGe layers during thermal treatment. Furthermore, the strained Si/SiGe layer may also be subjected to unwanted KOH etching if etching could not stop uniformly at the p^{++} SiGe etchstop layer due to variation of dopants in the p^{++} layer.

Another available technique for making SiGe-On-Insulator is via SIMOX as reported in a publication by T. Mizuno et al. entitled "High Performance Strained-Si p-MOSFETs on SiGe-on-Insulator Substrates Fabricated by SIMOX Technology," IEDM Technical Digest, 99-934, 1999. However, this method has limited applications because the oxygen implantation induces further damage in the relaxed SiGe layer in addition to the existing defects caused by lattice mismatch, which may consequently degrade the quality of the grown strained Si/SiGe. And, the high temperature anneal (>1100°C) needed to form oxide after the oxygen implantation is detrimental to the strained Si/SiGe layers since Ge tends to diffuse and agglomerate at temperatures above 600°C, this effect becomes more significant when the Ge content is higher than 10%. Furthermore, in this method, the insulator is limited to SiO_2 which has lower thermal conductivity compared to other insulators such as Al_2O_3.

Therefore, there is a need for an improved method for forming a structure suitable for growing strained epitaxial layers thereon.

SUMMARY OF THE INVENTION

This need is met by the invention claimed in claim 1.

In accordance with a preferred embodiment of the present invention, a method for forming a substrate suitable for growing high quality strained Si/SiGe layers on an insulator (SGOI) is described. This approach comprises the steps of selecting a first semiconductor substrate, forming

a first expitaxial graded layer of $Si_{1-x}Ge_x$ over the first semiconductor substrate, forming a second relaxed $Si_{1-y}Ge_y$ layer over the first graded layer, introducing hydrogen into the relaxed $Si_{1-y}Ge_y$ layer creating a hydrogen-rich defective layer comprising high density point defects and micro-cracks, the defective layer being within the relaxed $Si_{1-y}Ge_y$ layer, smoothing the surface of the relaxed SiGe epitaxial layer, selecting a second substrate having a layer of insulator such as SiO_2, Si_3N_4, Al_2O_3, or other acceptable or qualified low-k insulating materials, etc, on the second substrate, and having a planarized major surface on the second substrate, bonding the major surface of the first substrate to the major surface of the second substrate including the step of annealing to form a joined substrate pair with an insulator layer therein between, applying thermal treatments to the substrate pair to induce separation at the hydrogen-rich defective layer, the separation occurring to form a first structure containing the first substrate and a second structure containing the second substrate with a relaxed $Si_{1-y}Ge_y$ layer on insulator. The embodiment further includes smoothing the upper surface of the relaxed $Si_{1-y}Ge_y$ layer on said second substrate whereby the second structure is suitable for subsequent epitaxial growth of strained Si/SiGe layers for MOSFET, MODFET, HEMT or bipolar transistor device applications.

BRIEF DESCRIPTION OF THE DRAWING

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Fig. 1 is a cross section view of a first semiconductor substrate with an epitaxial layer of graded $Si_{1-x}Ge_x$ and a relaxed layer of $Si_{1-y}Ge_y$ covered with an encapsulation layer.

Fig. 2 is a cross section view of the first semiconductor substrate shown in Fig. 1 exposed to an ion bombardment of hydrogen resulting in a H-rich defective layer within the relaxed $Si_{1-y}Ge_y$ layer.

Fig. 3 is a cross section view of the first semiconductor substrate shown in Fig. 2 bonded to a second substrate with an insulator layer therein between.

Fig. 4 is a cross section view of separation at the H-rich defective layer within the relaxed $Si_{1-y}Ge_y$ layer during heat treatments, resulting in

transfer of a thin layer of relaxed $Si_{1-y}Ge_y$ or a plurality of layers containing the relaxed $Si_{1-y}Ge_y$ and the insulator layer from the first semiconductor substrate on to the second substrate shown in Fig. 3.

Fig. 5 is a cross section view of a first alternate embodiment of the invention having a smoothed surface of relaxed $Si_{1-y}Ge_y$ after Chemo-Mechanical Polishing (CMP).

Fig. 6 is a cross section view of a second alternate embodiment of the invention having a smoothed surface of relaxed $Si_{1-y}Ge_y$ after Chemo-Mechanical Polishing (CMP).

Fig. 7 is a cross section view of a thin layer of strained Si/SiGe grown on the upper surface of the embodiment shown in Fig. 5 with an optional thin layer of relaxed $Si_{1-y}Ge_y$ therein between.

Fig. 8 is a cross section view of a smoothed surface of the relaxed $Si_{1-y}Ge_y$ remaining on the first substrate after Chemo-Mechanical Polishing (CMP).

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The drawings illustrate the steps for the production of a thin layer of monocrystalline strained Si or strained SiGe on SiGe on insulator (SGOI) substrates with the aid of planarization of surfaces, wafer bonding and H-induced layer separation and transfer techniques.

Referring now to Fig. 1, a cross section view of a partial embodiment of the invention is shown comprising a substrate 10 and a plurality of layers 20, 30 and 40. Substrate 10 may be a single crystal material such as Si, SiGe, SiGeC, SiC, GaAs, InP, etc. suitable for forming epitaxial layers thereon. An epitaxial graded layer 20 of $Si_{1-x}Ge_x$ is formed on the upper surface 12 of substrate 10. The upper surface 22 of graded layer 20 is substantially relaxed or completely relaxed. The relaxation may be due to a modified Frank-Read mechanism described by LeGoues et al. in U.S. Pat. No. 5,659,187 which issued on Aug. 19, 1997 and is incorporated herein by reference. Formation of graded SiGe layer 20 may be formed as described in U.S. Pat. No. 5,659,187 by LeGoues et al. Layer 20 as well as layer 30 (to be described below) may be formed in a

UHV CVD process as described in U.S. Pat. No. 5,298,452 by B.S. Meyerson which issued Mar. 29, 1994 and is incorporated herein by reference. In layer 20, the concentration x of Ge may range from zero to a value in the range from 0.2 to 0.5. Layer 20 may have a thickness in the range from about 3,000 angstroms to 1000 nm.

Epitaxial layer 30 is comprised substantially or completely of relaxed $Si_{1-y}Ge_y$ and is formed on upper surface 22 of layer 20. Layer 30 may have a thickness in the range from 200nm to 1000nm. The Ge content y in layer 30 is chosen to match the crystal lattice constant of upper surface 22 of layer 20 such that layer 30 is relaxed or essentially strain free. The Ge content y in layer 30 may be equal to or about the value of x at upper surface 22. The value y may be in the range from about 0.2 to about 0.5. An encapsulation layer 40 may be formed over relaxed layer 30. Encapsulation layer 40 may be deposited via PECVD, LPCVD, UHV CVD or spin-on techniques. The encapsulation material may be, for example, Si, SiO_2, Poly Si, Si_3N_4, low-k dielectric materials, for example, Diamond Like Carbon (DLC), Fluorinated Diamond Like Carbon (FDLC), a polymer of Si, C, O, and H or a combination of any two or more of the foregoing materials. One example of a polymer of Si, C, O, and H is SiCOH described in US Serial No. 09/107567 filed Jun. 29, 1998 by Grill et al. entitled "Hydrogenated Oxidized Silicon Carbon Material" (Docket YOR919980245US1) which is incorporated herein by reference. The deposition temperature for forming layer 40 may be below 900°C. The thickness of the encapsulation layer is in the range from about 5nm to about 500nm. Encapsulation layer 40 functions to protect upper surface 32 of layer 30 or to provide an isolation layer.

Fig. 2 shows substrate 10 from Fig. 1 with SiGe epitaxial layers 20 and 30 and an encapsulation layer 40. Layers 40 and 30 are subjected to ion bombardment for the implantation of hydrogen ions 50. Hydrogen ions 50 may be H^+ or H_2^+ and preferably H_2^+. H_2^+ may be implanted at an energy in the range from about 30 KeV to about 200 KeV at a dose in the range from $3x10^{16}$ to $1x10^{17}$ ions/cm^2. The hydrogen implantation results in the formation of a H-rich layer 70. Layer 70 comprises hydrogen-containing SiGe point defects and planar micro cracks residing in principle crystallographic planes of SiGe. The energy of hydrogen ions 50 is selected to place the peak dose in layer 30 below surface 32 in the range from 100 nm to 1000 nm below surface 32. The hydrogen-rich SiGe layer 70 will form at the peak dose location of hydrogen.

After the step of implanting hydrogen, a second substrate 80 is bonded to layer 40. Prior to wafer bonding, surface 42 of layer 40 is polished by a Chemo-Mechanical Polishing (CMP) process to smooth surface 42 to a planar surface having a root mean square (RMS) in the range from .3 nm to 1 nm. Surface 42 may be polished before or after the step of implantation of hydrogen ions 50. Substrate 80 may be a semiconductor such as Si, SiGe, SiGeC or SiC; an insulator such as sapphire, glass or ceramic; or a metal and has an upper surface 90 which may be polished as above to provide a smooth upper surface 90 having a RMS in the range from about 0.3 nm to about 1 nm. The surface roughness or RMS may be determined by performing measurements with an Atomic Force Microscope (AFM) over an area of 20 x 20 microns.

The top surface 42 of layer 40 shown in Fig. 2 is turned upside down and brought into contact with surface 90 of substrate 80. The two surfaces 42 and 90 are brought together by the wafer bonding approach. Surfaces 42 and 90 are bonded together initially without affecting the integrity of layer 70. Layer 70 shall remain intact mechanically while surfaces 42 and 90 are bonded together by annealing at a temperature in the range from about 20°C to about 500°C for a time period in the range from about 2 hours to about 50 hours.

Layer 30 is then separated at layer 70 by annealing at a temperature in the range from 200 °C to 600 °C without disturbing the mechanical bond between surface 42 of layer 40 and surface 90 of substrate 80. Layer 30 when separated at layer 70 forms a new upper surface 75 of relaxed $Si_{1-y}Ge_y$ layer 74 which is the upper portion of layer 30, structure 82, after separation shown in Fig. 4. Also surface 73 of relaxed $Si_{1-y}Ge_y$ layer 72 is formed which is the lower portion of layer 30, structure 81, shown in Fig. 4. Layer 74, layer 40 and substrate 80 form SGOI which is structure 82 shown in Fig. 4. The thickness or depth of layer 74 is controlled by the ion bombardment energy such that surface 75 of layer 74 is away from the interface of layers 30 and 20 and therefore contains much less dislocation defects. Surface 75 of $Si_{1-y}Ge_y$ layer 74 with encapsulation layer 40 below may have a surface roughness in the range from about 3 nm to about 15 nm root mean square (RMS). Surface 75 is then smoothed with a Chemo-Mechanical Polishing (CMP) process. The Chemo-Mechanical Polishing (CMP) process may also be needed to thin down the SiGe for some specific applications, e.g., the SiGe may be thinned to a thickness in the range of

about 30nm to about 200nm for VLSI applications. The surface roughness of surface 75 after CMP is in the range from about 0.3 to about 1 nm RMS.

An example of a smoothing process for surface 75 of $Si_{1-y}Ge_y$ layer 74 by Chemical Mechanical Polishing (CMP) includes a slurry, a 1 psi down force, a 50 rpm of table speed, a 30 to 60 rpm carrier speed and a 0.5 psi backside air pressure. The polishing slurry may be SC112 commercially available from Cabot Corporation, Aurora, Illinois. The slurry flow rate may be 140 milliliters/minute. The polishing slurry may have a pH from about 9.5 to about 11.0. The weight % of solids, which contains silica or may be only silica, may be in the range from about 5% to about 30% (a greater range than is in SC112) and the silica particle size may be in the range from about 12 to about 200 nanometers (a greater range than is in SC112). The CMP may be performed in a Westech 372 polishing tool, which comprises a circular rotating polishing platen and a rotating wafer carrier.

The polishing pad system may be a two pad stacked system. The top pad may be product No. IC1000 and the subpad may be product No. Suba IV; both pads are commercially available from Rodel Corporation, Newark, Delaware. The top pad may be initially conditioned such as using a fixed abrasive (such as diamond) for 300 seconds before polishing. The pad is then conditioned for 25 seconds before each wafer is smoothed.

After the CMP process step, a brush cleaning step is performed. The brush cleaning is effective in removing residual abrasive particles from the wafer surface left from CMP. The brush cleaning step was performed using a conventional double-sided roller brush cleaner containing one stage of brush cleaning. The time duration of the roller brush cleaning step was 99 seconds.

After removing 100-300 nm of surface 75 of $Si_{1-y}Ge_y$ layer 74, the roughness (RMS) of epitaxially grown $Si_{1-y}Ge_y$ layer, where y is 0.15 i.e. 15% Ge, was reduced from 5-6nm to 0.5-0.8nm in Root-Mean-Squre (RMS), which is acceptable or qualified for epitaxial growth. With surface 75 of layer 74 smoothed and in condition for epitaxial growth thereon, Si or SiGe may be grown thereon by UHV CVD. Depending on the composition of the grown SiGe and the existing SiGe of layer 74, strained Si or SiGe is formed due to lattice mismatch determined by the difference in compositions.

Smoothing or planarization of SiGe for epitaxial growth has been shown in U.S. 6,107,653 by E.A. Fitzgerald in an epitaxial growth application on bulk silicon. In U.S. 6,107,653, chemo-mechanical polishing (CMP) of the upper surface of a graded SiGe layer was performed to remove the roughness created by dislocations introduced during relaxation of the SiGe layer. The planarization of the surface was for the purpose of preventing the continued roughening and grooving of the surface that leads to dislocation blocking. Planarization prevented a rise in the threading dislocation density during subsequent growth of the graded SiGe layer.

For a further description of CMP of SiGe and other materials to reduce surface roughness to below 1 nm RMS, reference is made to Serial No. 09/_____ by D.F. Canaperi et al. filed on even date of Sept. 29, 2000 entitled "A Method of Wafer Smoothing for Bonding Using Chemo-Mechanical Polishing (CMP)" which is assigned to the assignee herein and incoroporated herein by reference.

For a description of forming strained Si/SiGe for high speed CMOS devices reference is made to U.S. Pat. No. 5,534,713 by Ismail et al. which issued on July 9, 1996, U.S. Serial No. 09/267323 by Chu et al. (Docket YOR9-1999-0460US1) filed Mar. 12, 1999 which is assigned to the assignee herein and incorporated herein by reference and PCT Application No. US00/06258 by J.O. Chu (Docket YOR9-1999-0123PCT1) having a priority date of March 12, 1999 which is assigned to the assignee herein and incorporated herein by reference.

In an alternate embodiment, structure 82' includes substrate 80 with an insulator layer 83 between substrate 80 and layer 40 which is shown in Fig. 5. The insulator layer 83 may be deposited or formed via PECVD, LPCVD, UHV CVD, thermal oxidation or spin-on techniques. Insulator layer 83 may comprise a material selected from the group consisting of SiO_2, Si_3N_4, Al_2O_3, or other acceptable or qualified low-k dielectric materials, for example, Diamond Like Carbon (DLC), Fluorinated Diamond Like Carbon (FDLC), a polymer of Si, C, O, and H such as SiCOH or a combination of any two or more of the foregoing materials. The deposition temperature is below 900°C.

Insulator layer 83 may have an upper surface 84 which is polished via CMP in place of or in addition to surface 90 and may be bonded to upper surface 42 of layer 40. If insulator layer 40 is not present over relaxed $Si_{1-y}Ge_y$ layer 30 which after separation is layer 74, insulator layer 83 may be bonded directly to upper surface 32 of layer 74. The bonding steps for bonding insulator layer 83 to insulator layer 40 include annealing at a temperature in the range from about 20°C to about 500°C and for a time period in the range from about 2 hours to about 50 hours. The bonding steps for bonding insulator layer 83 to relaxed $Si_{1-y}Ge_y$ layer 30 include annealing at a temperature in the range from about 20 °C to about 500 °C and for a time period in the range from about 2 hours to about 50 hours.

In another embodiment, structure 82'' includes intermediate layer 86 formed with or in place of insulator layer 83. Fig. 6 shows layer 86 in place of layer 83 shown in Fig. 5. Layer 86 has an upper surface 87 bonded to surface 42 of layer 40. Intermediate layer 86 may be Ge, or metals which either have a low-melting point or react with silicon to form a silicide such as tungsten (W) or cobalt (Co) to achieve high bonding strength at anneal temperatures in the range from about 100°C to about 800°C. The anneal can be either a furnace anneal or a rapid thermal anneal (RTA). Depending on the selection of intermediate layer 86, the bonding interface can be between SiGe layer 74 and Ge or a metal or between the encapsulation layer 40 and Ge or a metal.

Fig. 7 shows a cross section view of structure 82''' including structure 82 shown in Fig. 4 with epitaxial layers 94 and 98 formed on upper surface 75 of layer 74. Layer 94 may be a thin layer in the range from about 30nm to about 500nm of relaxed epitaxial $Si_{1-y}Ge_y$ and layer 98 may be a thin layer in the range from about 100 angstroms to about 300 angstroms of strained Si. Field effect transistors for CMOS or MODFET's may be formed in strained Si layer 98. The strain in Si will be tensile and the mobility of holes and electrons will be increased due to the tensile strain.

Fig. 8 shows a cross section view of structure 81' shown in Fig. 4 with upper surface 73' smoothed after Chemo-Mechanical Polishing (CMP) to provide a relaxed $Si_{1-y}Ge_y$ surface suitable for epitaxial deposition of additional $Si_{1-y}Ge_y$ to rebuild the thickness of layer 72' back to the thickness of original layer 30 shown in Fig. 1 or to another selected

thickness. An additional layer 40 may be formed over surface 73' of layer 72' (not shown) to provide the embodiment shown in Fig. 1 for starting another sequence of steps as shown in Figs. 2-4. Alternatively, the embodiment shown in Fig. 8 may be used for starting another sequence of steps as shown in Figs. 2-4.

It should be noted in the drawing that like elements or components are referred to by like and corresponding reference numerals.

While there has been described and illustrated a method for forming strained Si or SiGe on SiGe on insulator (SGOI) using planarization, cleaning, bonding and layer separation by the implantation of hydrogen, it will be apparent to those skilled in the art that modifications and variations are possible without deviating from the broad scope of the invention which shall be limited solely by the scope of the claims appended hereto.

CLAIMS

1. A method of preparing a relaxed SiGe layer on an insulator, comprising the steps of forming a graded $Si_{1-x}Ge_x$ epitaxial layer on a first single crystalline semiconductor substrate, forming a relaxed $Si_{1-y}Ge_y$ epitaxial layer over the graded $Si_{1-x}Ge_x$ layer, forming a hydrogen-rich defective layer in the relaxed $Si_{1-y}Ge_y$ layer by hydrogen bombardment, providing a layer of an insulator over the surface of the relaxed $Si_{1-y}Ge_y$ layer, and separating the relaxed $Si_{1-y}Ge_y$ layer at the hydrogen-rich defective layer to form a first structure containing the first substrate, the graded $Si_{1-x}Ge_x$ layer and a relaxed $Si_{1-y}Ge_y$ layer, and a second structure containing the insulator layer with a relaxed $Si_{1-y}Ge_y$ layer on its surface.

2. The method of claim 1, wherein the step of providing a layer of an insulator over the surface of the relaxed $Si_{1-y}Ge_y$ layer comprises selecting a second substrate having an insulator layer thereon, and bonding the surface of the relaxed $Si_{1-y}Ge_y$ epitaxial layer on the first substrate to the surface of the insulator layer on the second substrate, whereby the second structure contains the second substrate and the insulator layer with the relaxed $Si_{1-y}Ge_y$ layer on its surface.

3. The method of claim 1, wherein the step of providing a layer of an insulator over the surface of the relaxed $Si_{1-y}Ge_y$ layer comprises forming an insulator layer thereon, the method further comprising selecting a second substrate, and bonding the second substrate to the insulator layer, whereby the second structure contains the second substrate and the insulator layer with the relaxed $Si_{1-y}Ge_y$ layer on its surface.

4. The method of any preceding claim, further including the step of growing an epitaxial layer on the surface of the relaxed $Si_{1-y}Ge_y$ layer of the second structure.

5. The method of claim 4, wherein the epitaxial layer is a strained layer.

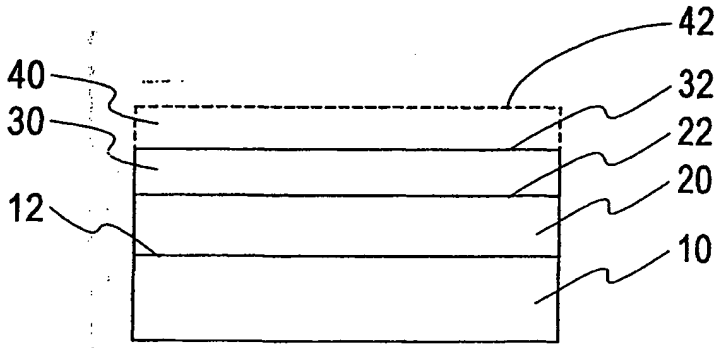

Fig. 1

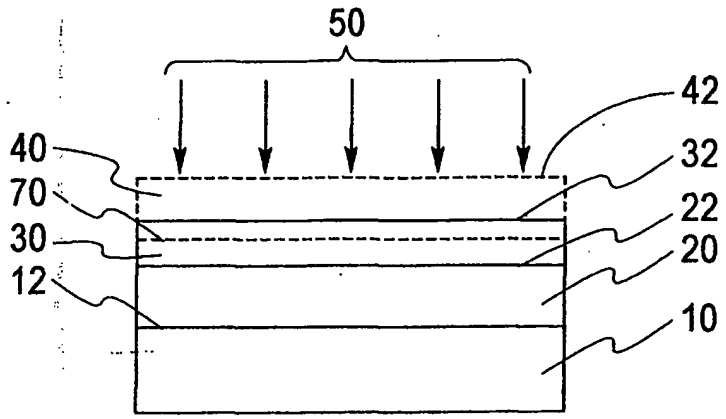

Fig. 2

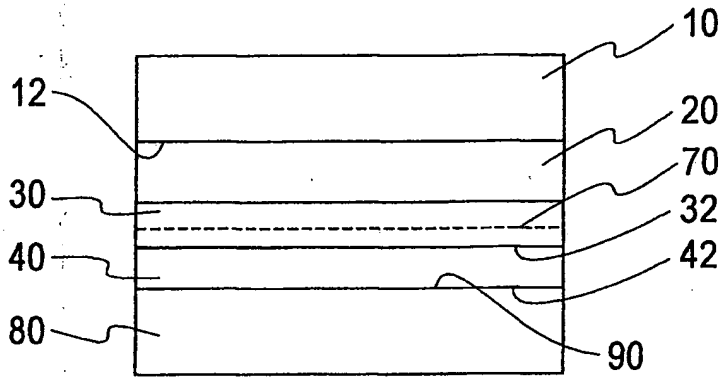

Fig. 3

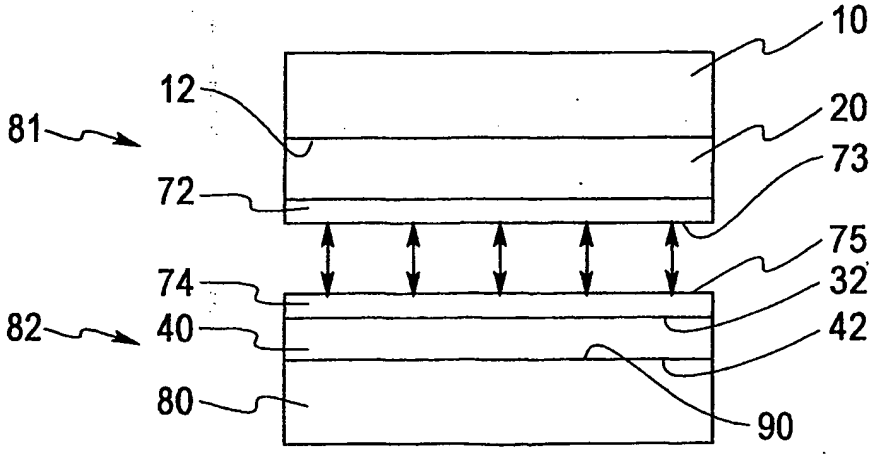

Fig. 4

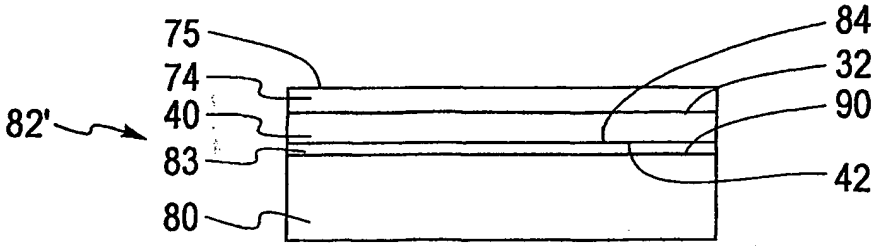

Fig. 5

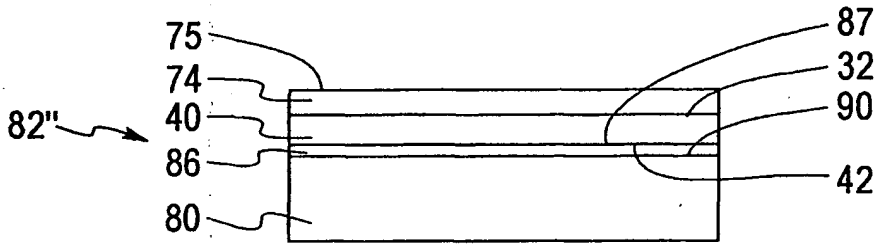

Fig. 6

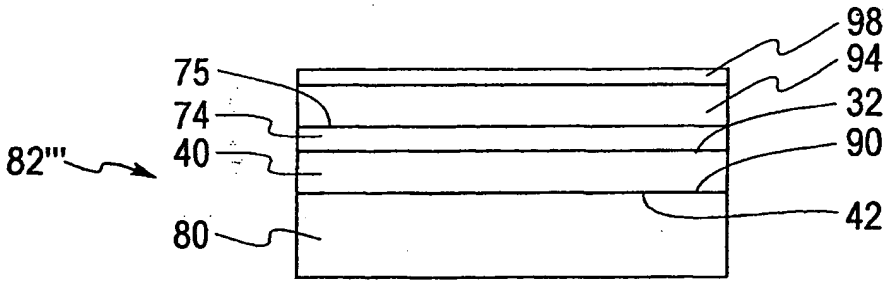

Fig. 7

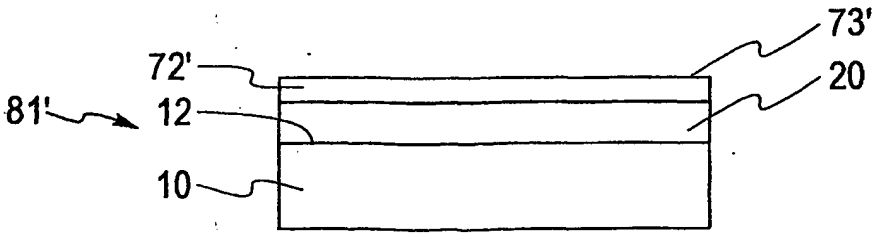

Fig. 8

INTERNATIONAL SEARCH REPORT

In I Application No
PCT/GB 01/04321

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/762 H01L21/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 882 987 A (SRIKRISHNAN KRIS V) 16 March 1999 (1999-03-16) cited in the application column 4, line 8 -column 6, line 10; figures 4,5	1-3
A	MIZUNO T ET AL: "High performance strained-Si p-MOSFETs on SiGe-on-insulator substrates fabricated by SIMOX technology" ELECTRON DEVICES MEETING, 1999. IEDM TECHNICAL DIGEST. INTERNATIONAL WASHINGTON, DC, USA 5-8 DEC. 1999, PISCATAWAY, NJ, USA,IEEE, US, 5 December 1999 (1999-12-05), pages 934-936, XP010372110 ISBN: 0-7803-5410-9 cited in the application the whole document	1,4,5

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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Date of the actual completion of the international search	Date of mailing of the international search report
8 February 2002	22/02/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Klopfenstein, P

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
P,A	HUANG L J ET AL: "SIGE-ON-INSULATOR PREPARED BY WAFER BONDING AND LAYER TRANSFER FOR HIGH-PERFORMANCE FIELD-EFFECT TRANSISTOR" APPLIED PHYSICS LETTERS, AMERICAN INSTITUTE OF PHYSICS. NEW YORK, US, vol. 78, no. 9, 26 February 2001 (2001-02-26), pages 1267-1269, XP001020601 ISSN: 0003-6951 page 1267; figure 1	1-5

INTERNATIONAL SEARCH REPORT

Information on patent family members

In nal Application No
PCT/GB 01/04321

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5882987 A	16-03-1999	JP 3037934 B2	08-05-2000
		JP 11121377 A	30-04-1999